IN THE CLAIMS

The listing of the claims will replace all prior versions and listings of the claims in the application:

1.-68. (Canceled)

69. (new) A semiconductor chip, comprising:

a) a multi-ported memory having a plurality of data input ports;

b) a controller to execute test commands to test said multi-ported memory; and,

c) an interface circuit to interface said data input ports to both said controller and a system that uses said memory, said interface circuit comprising a group of three circuit paths for each one of said memory input ports, each circuit path of said group of three circuit paths to transport data to be written into said memory, each said group of three circuit paths comprising:

i) a first circuit path that flows from said system to a data input port that said first circuit path's group of three circuit paths are associated with, said first circuit path to transport data provided by said system;

ii) a second circuit path that flows from said controller to said data input port, said second circuit path to transport first test data provided by said controller;

iii) a third circuit path that flows from said controller to register circuitry and from said register circuitry to said data input port, a portion of said third circuit path that precedes said register circuitry to transport second test data provided by said controller, a portion of said third circuit path that follows said register circuitry to transport said second test data after it has already been transported into said memory by another group's second circuit path.

70. (new) The semiconductor chip of claim 69 wherein said interface circuit further comprises a multiplexer comprising:

a) a channel select input coupled to an output of said controller;

b) an input through which only one of said circuit paths flow; and,

c) an output through which more than one of said circuit paths flow.

71. (new) The semiconductor chip of claim 69 wherein said test commands comprise a PRELOAD WRITE command.

72. (new) The semiconductor chip of claim 69 wherein said test commands comprise a PRELOAD READ command.

73. (new) The semiconductor chip of claim 69 wherein said test commands comprise a WRITE command.

74. (new) The semiconductor chip of claim 73 wherein said WRITE command has a field to indicate less than a full word is to be written.

75. (new) The semiconductor chip of claim 69 wherein said test commands comprise a READ command.

76. (new) The semiconductor chip of claim 75 wherein said READ command has a field to indicate less than a full word is to be read.

77. (new) The semiconductor chip of claim 69 wherein said controller comprises an output to send a command to a downstream controller in a daisy chain configuration.

78. (new) The semiconductor chip of claim 77 wherein said controller comprises a transparent mode in which test commands received by said controller are:

not executed by said controller; and,

forwarded to said downstream controller.

79. (new) The semiconductor chip of claim 78 wherein said controller comprises a selected mode in which test commands received by said controller are executed by said controller.

80. (new) The semiconductor chip of claim 79 wherein said controller, while in said selected mode, also forwards received test commands to said downstream controller.

81. (new) A method, comprising:

(i) while testing a multi-ported memory:

a) issuing test data from a controller to be written into said multi-ported memory:

from at least one data input port of said multi-ported memory, but not, from all data input ports of said multi-ported memory;

b) writing said test data into said multi-ported memory from said at least one data input port of said multi-ported memory, and, for each of said data input ports of said multi-ported memory that said writing is not applied to:

storing said test data into register circuitry;

c) for at least one of said data input ports of said multi-ported memory that said writing is not applied to:

reading said test data from said register circuitry, and,

writing said test data into said multi-ported memory from said at least one data input port of said data input ports that said writing of b) was not applied to; and,

(ii) while operating a system that uses said multi-ported memory:

writing data into a particular data input port of said multi-ported memory, said data flowing through a multiplexer through which said test data flowed

prior to said test data being said written into said multi-ported memory from said particular data input port.

82. (new) The method of claim 81 wherein said at least one of said data input ports that said writing of b) was not applied to further comprises all of said data input ports that said writing of b) was not applied to.

83. (new) The method of claim 81 further comprising:

sending test commands to said controller;

sending said test commands from said controller to a next controller in a daisy chain configuration;

using said test commands to test a second multi ported memory that said next controller is coupled to.

84. (new) The method of claim 83 wherein said testing of said second multi-ported memory further comprises:

d) issuing second test data from said next controller to be written into said second multi-ported memory:

from at least one data input port of said second multi-ported memory, but not,

from all data input ports of said second multi-ported memory;

e) writing said second test data into said second multi-ported memory from said at least one data input port of said second multi-ported memory,

and, for each of said data input ports of said second multi-ported memory that said writing is not applied to:

storing said test data into second register circuitry; and,

f) for at least one of said data input ports of said second multi-ported memory that said writing of e) is not applied to:

reading said second test data from said second register circuitry, and,

writing said second test data into said second multi-ported memory from said at least one data input port of said data input ports that said writing of e) was not applied to.

85. (new) The method of claim 84 further comprising, while operating a system that uses said second multi-ported memory, writing second data into a particular data input port of said second multi-ported memory, said second data flowing through a second multiplexer through which said second test data flowed prior to said second test data being said written into said second multi-ported memory from said particular data input port.

86. (new) The method of claim 84 further comprising sending a command to said controller prior to said sending test commands to said controller that cause said controller to enter a transparent mode and not execute said test commands.

COMMENTS

The enclosed is responsive to the Examiner's Final Office Action mailed on May 12, 2004 and is being filed pursuant to a Request for Continued Examination (RCE) as provided under 37 CFR 1.114. The claims of the present application have been amended as follows: 1) claims 1, 3-9, 13-28, 30-36, 39, 41-52 and 54-68 have been canceled; and, 2) new claims 69 - 86 have been added. The Applicant respectfully requests reconsideration of the present application and the allowance of claims 69 - 86.

In light of the Applicant's claim amendments the Examiner's stated reasons of rejection as provided in the Final Office Action mailed on 5/12/04 are presently moot.

For guidance in understanding new independent claims 69 and 84, the Examiner's attention is drawn to paragraphs 0034 – 0037 of the present application which makes reference to the circuitry and operation of interface circuit 258 of Figure 2 of the present application.

The Applicant respectfully submits that independent claims 69 and 84 are allowable over the prior art of record because the prior art of record fails to disclose, teach or suggest – when viewing the prior art items of record alone or combination with one another – to suggest the subject matter presently being claimed by claims 69 and 84.